WHAT IS CLAIMED IS:

1. A method for changing a phase of a clock signal, the method comprising:

generating N clock signals that each have a period, wherein each of the N clock signals has the same period and a different phase;

selecting first and second ones of the N clock signals to provide a selected clock signal and a phase forward clock signal using selection circuits; and

in response to a phase change signal, shifting the phase of the selected clock signal and the phase forward clock signal by causing the selection circuits to select different ones of the N clock signals.

2. The method of claim 1 further comprising:

dividing the frequency of the selected clock signal by a fractional value to generate an output clock signal, a frequency of the output clock signal being 1/M times the frequency of one of the N clock signals, wherein M is not a whole number

3. The method of claim 1 wherein dynamically shifting the phase of the selected clock signal by 360°/N in response to a phase change signal further comprises shifting phases of the selected clock signal and the phase forward clock signal backward by 360°/N on an edge of the selected clock signal, and shifting the phases of the selected clock signal and the phase forward clock signal forward by 360°/N on an edge of the phase forward clock signal.

4. The method of claim 3 wherein shifting the phases of the selected clock signal and the phase forward clock signal further comprises:

changing values of first and second select signals in response to the phase change signal;

selecting a different one of the N clock signals to shift the phase of the selected clock signal in response to the changed value of the first select signal; and

selecting a different one of the N clock signals to shift the phase of the phase forward clock signal in response to the changed value of the second select signal.

5. The method of claim 4 wherein the first and the second select signals are count signals, the phase of the selected clock signal and the phase forward clock signal shifting forward by 360°/N when the first and the second select signals increase, the phase of

the selected clock signal and the phase forward clock signal shifting backward by 360°/N when the first and the second select signals decrease.

6. The method of claim 4 wherein binary values of the first and the second select signals are shifted in one direction to increase the phases of the selected clock signal and the phase forward clock signal by 360°/N, and the binary values of the first and the second select signals are shifted in a second direction to decrease the phases of the selected clock signal and the phase forward clock signal by 360°/N.

7. A method for changing a phase of an output clock signal, the method comprising:

providing first and second clock signals having different phases;

in response to a phase change signal, shifting the phases of the first and the second clock signals backward on an edge of the first clock signal;

in response to the phase change signal, shifting the phases of the first and the second clock signals forward on an edge of the second clock signal; and

providing the first clock signal as the output signal.

8. The method of claim 7 further comprising:

generating N clock signals using an oscillator, phases of the N clock signals being separated by 360°/N, and a period of each of the N clock signals having the same length,

wherein the first clock signal is selected from among the N clock signals using a first multiplexer, and the second clock signal is selected from among the N clock signals using a second multiplexer.

9. The method of claim 8 wherein the phases of the first and the second clock signals are shifted backward when a directional signal is a first value, and the phases of the first and the second clock signals are shifted forward when the directional signal is a second value.

10. The method of claim 9 wherein:

shifting the phases of the first and the second clock signals forward and backward further comprises changing a value of first and second count signals in a direction indicated by the directional signal, providing the first count signal to the first multiplexer, and providing the second count signal to the second multiplexer.

11. The method of claim 9 wherein shifting the phases of the first and the second clock signals forward and backwards further comprises:

generating first digital select signals that indicate to the first multiplexer which of the N clock signals to select;

generating second digital select signals that indicate to the second multiplexer which of the N clock signals to select;

causing a HIGH signal within each of the first and the second count signals to shift to a different bit position in response to the phase change signal;

changing the phase of the first clock signal by selecting a different one of the N clock signals using the first multiplexer in response to changes in the first digital select signals; and

changing the phase of the second clock signal by selecting a different one of the N clock signals using the second multiplexer in response to changes in the second digital select signals.

12. A phase shift selection circuit comprising:

a first multiplexer that selects one of N clock signals that have different phases to provide an output clock signal;

a second multiplexer that selects one of the N clock signals to provide a phase forward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N; and

a phase shift selection circuit that dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

13. The phase shift selection circuit according to claim 12 further comprising:

a voltage controlled oscillator coupled to the first and the second multiplexers that generates the N clock signals.

14. The phase shift selection circuit according to claim 12 further comprising:

an adjustable delay circuit coupled to the first and the second multiplexers that generates the N clock signals.

15. The phase shift selection circuit according to claim 12 further comprising:

a frequency divider that divides the frequency of the output clock signal by a fractional value.

16. The phase shift selection circuit according to claim 12 further comprising:

a third multiplexer that selectively couples the output clock signal and the phase forward signal to an input of the phase selection circuit.

17. The phase shift selection circuit according to claim 12 wherein the phase shift selection circuit increases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the phase forward signal when a directional signal is a first value, and the phase shift selection circuit decreases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the output clock signal when a directional signal is a second value.

18. The phase shift selection circuit according to claim 12 wherein the phase shift selection circuit is a counter circuit that generates first and second count signals that control the first and the second multiplexers, respectively, values of the first and the second count signals changing in response to the phase change signal.

19. The phase shift selection circuit according to claim 12 wherein the phase shift selection circuit is a cyclic shift register that generates a first set and a second set of digital signals that control the first and the second multiplexers, respectively, values of the first and the second sets of digital signals shifting in response to the phase change signal.

20. A phase shift selection circuit comprising:

a first multiplexer that selects one of a plurality of clock signals to provide an output clock signal, each of the clock signals having a different phase;

a second multiplexer that selects one of the clock signals to provide a phase forward clock signal; and

a multiplexer control circuit that decreases phases of the output and the phase forward clock signals on an edge of the output clock signal, and increases the phases of the

output and the phase forward clock signals on an edge of the phase forward clock signal in response to a phase change signal.

21. The phase shift selection circuit of claim 20 further comprising:

an oscillator coupled to the first and the second multiplexers that generates the clock signals.

22. The phase shift selection circuit of claim 20 further comprising:

a delay circuit coupled to the first and the second multiplexers that generates the clock signals.

23. The phase shift selection circuit of claim 20 wherein the multiplexer control circuit is a counter circuit that generates a first count signal at the first output and a second count signal at the second output, the first and the second count signals changing in response to the phase change signal.

24. The phase shift selection circuit of claim 20 further comprising:

an output counter circuit that divides the frequency of the output clock signal by a fractional value.

25. The phase shift selection circuit of claim 20 wherein the multiplexer control circuit is a cyclic shift register that generates first and second sets of digital signals, values of the first and the second sets of digital signals shifting in response to the phase change signal.

26. The phase shift selection circuit of claim 20 further comprising:

a third multiplexer coupled to receive the output clock signal and the phase forward clock signal from the first and the second multiplexers, the third multiplexer having an output coupled to an input of the multiplexer selection circuit.

27. The phase shift selection circuit of claim 20 wherein the multiplexer control circuit decreases the phases of the output and the phase forward clock signals when a phase direction signal is a first value, and the multiplexer control circuit increases the phases of the output and the phase forward clock signals when the phase direction signal is a second value.

28. A method for changing a phase of a clock signal, the method comprising:

generating N clock signals that each have a period, wherein each of the N clock signals has the same period and a different phase;

selecting a first one of the N clock signals to provide a selected clock signal using a multiplexer circuit;

changing a voltage of a phase change signal while the multiplexer circuit is ON; and

in response to the changed voltage of the phase change signal, shifting the phase of the selected clock signal by causing the multiplexer to select a different one of the N clock signals, wherein shifting the phase of the selecting clock signal does not cause glitches in the selected clock signal.

29. A delay locked loop circuit comprising:

a delay circuit that generates N clock signals that have different phases;

a first multiplexer coupled to the delay circuit that selects one of the N clock signals to provide an output clock signal;

a second multiplexer coupled to the delay circuit that selects one of the N clock signals to provide a phase forward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N; and

a phase shift selection circuit that dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

30. The delay locked loop circuit of claim 29 wherein the phase shift selection circuit is a counter circuit that generates first and second count signals that control the first and the second multiplexers, respectively, values of the first and the second count signals changing in response to the phase change signal.

31. The delay locked loop circuit of claim 29 wherein the phase shift selection circuit is a cyclic shift register that generates a first set and a second set of digital signals that control the first and the second multiplexers, respectively, values of the first and the second sets of digital signals shifting in response to the phase change signal.

32. A phase locked loop circuit comprising:

an oscillator that generates N clock signals that have different phases;

a first multiplexer coupled to the oscillator that selects one of the N clock signals to provide an output clock signal;

a second multiplexer coupled to the oscillator that selects one of the N clock signals to provide a phase forward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N; and

a phase shift selection circuit that dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

33. The phase locked loop circuit of claim 32 wherein the phase shift selection circuit increases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the phase forward signal when a directional signal is a first value, and the phase shift selection circuit decreases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the output clock signal when a directional signal is a second value.